IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF ILLINOIS
EASTERN DIVISION

HFT SOLUTIONS, LLC, *Plaintiff*, v. CITADEL SECURITIES LLC, *Defendant*.	Case No. 1:24-cv-13213

PLAINTIFF HFT SOLUTIONS' RESPONSE IN OPPOSITION TO
DEFENDANT CITADEL SECURITIES' MOTION TO DISMISS

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I. INTRODUCTION

Defendant's motion is a transparent attempt to stall this case, not a serious challenge to patent-eligibility. Defendant fundamentally relies on a gross oversimplification—ignoring numerous limitations of the claims and disclosures in the specification—to improperly recast the asserted patents as generic data-clock synchronization or "mere data manipulation." Under any faithful reading, however, the claims and specification describe innovative FPGA systems and methods that improve over conventional systems in specific, concrete ways.

The patents describe, for example, an FPGA system comprising: a deserializer that generates a receiver side clock signal and transmits it to an external phase lock loop (PLL), where the deserializer is in an FPGA, the external PLL is not within the FPGA, and a transmitter side clock signal is derived from a clock signal generated by the external PLL. These and other aspects of the claimed inventions help reduce latency by, for example, eliminating conventional clock-domain-crossing (CDC) circuitry and operations that were used to synchronize clock signals in prior art systems. The Federal Circuit has consistently found technical advances like these patent-eligible. Thus, accepting the allegations in the complaint and patents as true and drawing all inferences in Plaintiff's favor, the patents are nowhere near the threshold for patent-ineligibility.

At minimum, the Court should defer ruling on patent eligibility until after the claims are construed and a sufficient factual record developed. The patents carry a presumption of validity that can only be overcome with clear and convincing evidence. Defendant's distortion of the patents at most raises factual disputes that foreclose dismissal.[1]

Defendant's motion should be denied.

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[1] Notably, in a related case on the same patents, that defendant did not move to dismiss and chose instead to answer the complaint. *See HFT Solutions, LLC v. Jump Trading, LLC*, No. 1:24-cv-13214 (N.D. Ill.), ECF No. 28.

II. FACTUAL BACKGROUND

A. The Asserted Patents Provide Specific Technical Improvements Over Conventional FPGA Systems

The asserted patents are related and share the same specification. Dkt. 1 ¶¶ 2-4, Exs. 1-3. The patents explain that "FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired." '381 patent (Dkt. 1-3) 1:39-43.[2] As shown below, the patents go on to identify specific technical problems with conventional FPGAs and explain why prior art attempts to solve them were inadequate.

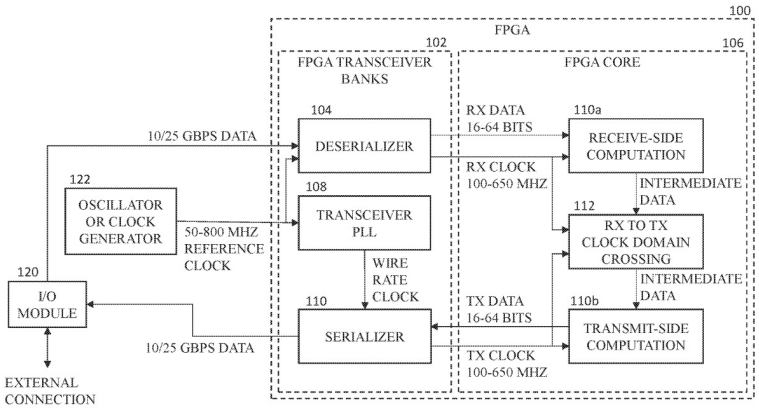
1. Exemplary Technical Problems Described in the Specification

"One technological problem with FPGAs is that there is a need to synchronize receiving side and transmitting side clock signals within the FPGA." *Id*. 1:43-47. "The prior art sought to address this problem by including a [CDC] circuit in the FPGA, however, these circuits inherently add a delay to the processing" and in "high frequency trading … even small delays may present a large problem." *Id*. 1:47-52. "Accordingly, a technical problem is presented in FPGAs in that phase synchronization between the receiver side clock and the transmitter side clock will introduce unwanted latency that results in delay of processing." *Id*. 1:53-56.

The patents are directed to solving these and other "technological challenges" in conventional FPGAs. '381 patent 1:66-7:53. Referring to Fig. 1 below, for example, the patents explain that in conventional systems, "a REFERENCE CLOCK signal is provided, by Oscillator or Clock Generator 122, to both the deserializer 104 and the serializer 110." *Id*. 10:16-18. This leads to timing issues because the receiver and transmitter side clocks (RXCLOCK and TX CLOCK) differ in both frequency and phase based on the deserialization and serialization

[2] For ease of reference, Plaintiff cites only the '381 patent to refer to specific passages in the shared specification. Corresponding disclosures can be found in the '286 and '305 patents.

processes occurring in the deserializer 104 and serializer 110. *Id*. 10:20-28. "As a result, the RXCLOCK signal and TXCLOCK signal will be out of phase." *Id*.



PRIOR ART
FIG. 1

('381 Fig. 1)

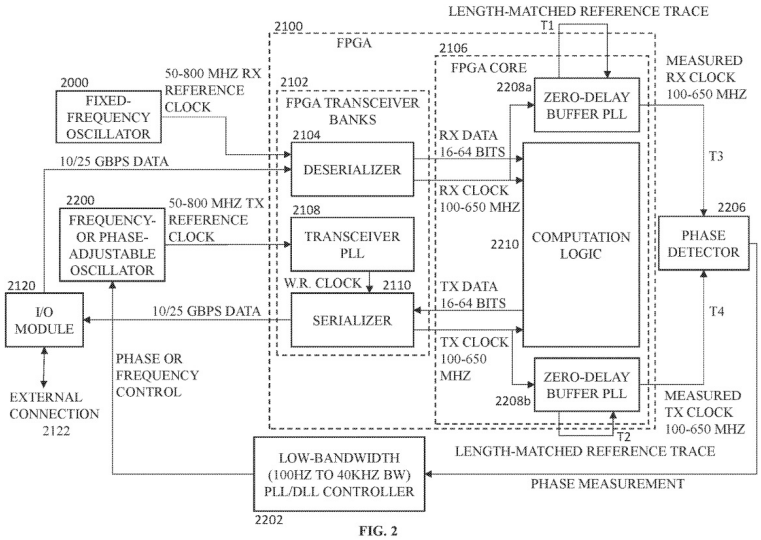
Conventional solutions used to address this issue, such as "the inclusion of the RX to TX clock domain crossing circuit 112" (*Id*. 10:28-29) "creates a technical problem, introducing an inherent delay in the FPGA 100." *Id*. 10:33-35; *see also* 11:3-8 (CDC 112 "adds latency related to the phase difference … plus the latency of the synchronizers … and does not perform any computation, such that it slows the effective processing speed of FPGA 100.").

2. Exemplary Technical Solutions Taught by the Specification

The patents disclose specific technological improvements to address these problems. Referring to Fig. 2 below, in some embodiments, a phase controller 2202 that is external[3] to FPGA 2100, "provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK." *Id*. 13:51-60. The controller "utilizes a phase-locked loop" (PLL) and monitors the phase offset between RXCLOCK and TXCLOCK using, e.g., phase detector 2206

[3] This technical solution uses an external circuit since, at the time of the invention – and even today – conventional FPGA's use clock domain crossing circuits instead of a PLL phase controller like the patents.

and zero-delay buffers 2208a and 2208b. *Id*. 13:51-14:36, 15:61-62. Based on the phase offset, controller 2202 sends control signals to adjustable oscillator 2200 which generates a wire rate clock signal W.R. CLOCK. Serializer 2110 within FPGA 2100 derives TXCLOCK from W.R. CLOCK and transmits TXCLOCK to computation logic 2210. *Id*. 12:63-13:9, 13:51-14:36.



('381 Fig. 2)

This exemplary configuration solves the added latency problem caused by conventional CDC circuits. *Id*. 14:37-47. ("Using the configuration of FIG. 2, [RXCLOCK and TXCLOCK] are sufficiently aligned in phase such that there is no need for the [CDC] circuit discussed above, eliminating a technical problem."); *see also id*. 14:47-52 ("Some delays may be introduced in the path … however, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.").

3. Exemplary Technical Solutions Recited in the Claims

The claims of the patents capture the specific technological improvements discussed in the specification, including those above. As the Complaint alleges, the claims "recite technical solutions to technical problems related to, for example, processing delays caused by clock domain crossing circuits, and phase synchronization between receiver and transmitter side clocks." Dkt. 1 ¶ 19. For example, at least the claim 1 elements highlighted for each patent in Exhibit 1

describe key aspects of these technical solutions which help eliminate CDC circuits and operations (and the latency and processing delay that they cause) used in conventional FPGA systems.

B. Defendant Benefits from the Technical Solutions in the Claimed Inventions

As alleged in Plaintiff's Complaint, Defendant "is a trading firm engaged in various high frequency trading strategies" that "fundamentally rely on being able to execute trades faster, sometimes microseconds or nanoseconds faster, than competitors." Dkt. 1 ¶ 6. To secure that speed advantage, Defendant configures and uses the accused FPGA systems in a manner that infringes the asserted patents. *Id*. ¶¶ 7-8, Exs. 4-6. Defendant's infringement yields increased profits on its latency-sensitive trading activities. *Id*. ¶ 25 ("Defendant and its customers derive benefits from Defendant's infringement including, for example, higher success rates and increased profits in latency sensitive trades … and other trading activities affected by latency.").

III. LEGAL STANDARD

Deciding a § 101 challenge requires determining: "(1) whether the claim, as a whole, is 'directed to' patent-ineligible matter—here, an abstract idea—and (2) if so, whether the elements of the claim, considered individually or as an ordered combination 'transform the nature of the claim' into a patent-eligible application." *Ancora Techs., Inc. v. HTC Am., Inc.*, 908 F.3d 1343, 1347 (Fed. Cir. 2018) (citing *Alice Corp. Pty. v. CLS Bank Int'l*, 573 U.S. 208, 216-17 (2014)).

The first step (1) examines the claims "in light of the specification" to determine if "their character as a whole is directed to excluded subject matter." *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1334 (Fed. Cir. 2016). Claims should not be "oversimplified" and their benefits not "downplayed." *Id*. at 1337-38. For "all inventions at some level embody, use, reflect, rest upon, or apply laws of nature, natural phenomena, or abstract ideas." *Core Wireless Licensing S.A.R.L. v. LG Elecs., Inc.*, 880 F.3d 1356, 1361 (Fed. Cir. 2018) (quotations omitted).

If a claim is directed to an abstract idea, courts proceed to step two (2) to "determine whether it contains an 'inventive concept' sufficient to 'transform' the claimed abstract idea into patent-eligible application." *Alice*, 573 U.S. at 221. Although individual elements may be conventional, their specific arrangement can form an inventive concept. *Bascom Glob. Internet Servs., Inc. v. AT&T Mobility LLC*, 827 F.3d 1341, 1349 (Fed. Cir. 2016). A claim is ineligible under step two if it involves nothing more than "well-understood, routine, [and] conventional activities previously known to the industry." *Alice*, 573 U.S. at 225. This determination is "a question of fact" and thus requires clear and convincing evidence. *Berkheimer v. HP Inc.*, 881 F.3d 1360, 1368 (Fed. Cir. 2018) ("Any fact, such as this one, that is pertinent to the invalidity conclusion must be proven by clear and convincing evidence.").

IV. ARGUMENT

Defendant's motion collapses at *Alice* step one. The asserted claims are not directed to an abstract idea, but rather to specific FPGA system architectures that solve technical problems in conventional systems with an inventive, unconventional technological solution. Even if the Court proceeds to step two, the motion still fails. Defendant offers no clear and convincing evidence that the claimed arrangements, including the absence of CDC circuits and operations in both the claims and the infringing FPGA systems, were "well-understood, routine, and conventional." Moreover, step-two eligibility turns on questions of fact that cannot be resolved on the pleadings.

A. Defendant Fails to Show the Asserted Patents Are Directed to an Abstract Idea

1. Defendant's Oversimplification Invites Reversible Error

Defendant's abstract-idea argument rests on the very approach the Federal Circuit has repeatedly condemned—reducing the claims to a generic, high-level summary untethered from what they actually recite. *See Contour IP Holding LLC v. GoPro, Inc.*, 113 F.4th 1373, 1379 (Fed. Cir. 2024) ("[W]e must avoid describing the claims at a high level of abstraction, divorced from

the claim language itself."); *see also TecSec, Inc. v. Adobe Inc.*, 978 F.3d 1278, 1294 (Fed. Cir. 2020) ("[A]ccurate characterization of what the claims require and of what the patent asserts to be the claimed advance" is "crucial" to the step one analysis).

By reducing the claims to generic notions such as "synchronizing data processing with a clock" or "mere data manipulation" (Mot. 6), Defendant impermissibly "disregard[s] elements of the claims at issue that the specification makes clear are important parts of the claimed advance in the combination of elements." *TecSec*, 978 F.3d at 1294 (claims directed to improvements in "secure and efficient data transmission" not abstract). For example, Defendant simply ignores specially configured components such as: a deserializer that receives a clock signal, generates a receiver side clock signal, transmits the receiver side clock signal to a PLL external to the FPGA, and transmits parallel data streams to computation circuitry in the FPGA; and the external PLL itself, which generates a second clock signal from which a transmitter side clock signal is derived within the FPGA.[4] Defendant's oversimplification and stripping of claim language is evident from its "summary" of claim 1 of each patent alone, which omits essentially all critical claim language. *Compare* Mot. at 6 *with* Ex. 1. *See Packet Intel. LLC v. NetScout Sys., Inc.*, 965 F.3d 1299, 1308-10 (Fed. Cir. 2020) (rejecting defendants' oversimplification of the claims as being directed to "collection, comparison, and classification of information" and upholding eligibility of claims reciting specific steps for improving classification of network traffic).

Accurately characterized, the claimed inventions here provide tangible improvements to FPGA system designs—not generic "data manipulation" or basic clock-syncing—and are plainly

[4] Throughout this brief, Plaintiff summarizes claim elements and patent disclosures solely for purposes of demonstrating that Defendant's § 101 challenge is baseless. These summaries pertain to exemplary features and should not be taken out of context or used as purported summaries of all claims of all patents or of any individual claimed invention as a whole, including for example, in any *inter partes* review (IPR) petitions or claim construction briefs that Defendant may file.

not abstract. "Indeed, some improvements in computer-related technology when appropriately claimed are undoubtedly not abstract, such as a chip architecture." *Enfish*, 822 F.3d at 1335. As discussed above, the claimed inventions describe specific FPGA system architectures that, for example, eliminate the need for conventional CDC circuits and the latency and processing delays caused by such extra circuitry. *See* Factual Background; *see also* Ex. 1. As the Complaint alleges, the claims provide "technical solutions to technical problems related to, for example, processing delays caused by clock domain crossing circuits, and phase synchronization between receiver and transmitter side clocks." Dkt. 1 ¶ 19.

2. Federal Circuit Precedent Confirms Eligibility

The Federal Circuit consistently upholds patent-eligibility at *Alice* step one where, as here, the claims are necessarily rooted in computer technology in order to solve specific technical problems in computer functionality. *Ancora* upheld eligibility of claims directed to improving computer security as non-abstract because the claimed technique "departs from earlier approaches to solve a specific computer problem." *Ancora Techs. Inc. v. HTC America, Inc.*, 908 F.3d 1343, 1348 (Fed. Cir. 2018). *Uniloc* ruled that claims "directed to a patent-eligible improvement to computer functionality, namely the ***reduction of latency*** experienced … in communication systems" were not abstract. *Uniloc USA, Inc. v. LG Elecs. USA, Inc.*, 957 F.3d 1303, 1306, 1307 (Fed. Cir. 2020). *DDR* found claims non-abstract because "the claimed solution is necessarily rooted in computer technology in order to overcome a problem specifically arising in the realm of computer networks." *DDR Holdings, LLC v. Hotels.com, L.P.*, 773 F.3d 1245, 1257 (Fed. Cir. 2014). *SRI* likewise held that claims "necessarily rooted in computer technology in order to solve a specific problem in the realm of computer networks" were not abstract. *SRI Int'l, Inc. v. Cisco Sys., Inc.*, 930 F.3d 1295, 1303 (Fed. Cir. 2019).

Applying this binding precedent, courts in this district have likewise found computer-related claims directed to specific technological improvements not abstract. For example, in *Buffalo Pats., LLC v. Motorola Mobility LLC*, the court denied a motion to dismiss where the claims were "directed to a technical improvement in conventional message recognition technology, not an abstract idea." No. 22-CV-04540, 2023 WL 5858921 at *3 (N.D. Ill. Sept. 11, 2023). The court found that, as here, the specification identified shortcomings in prior art systems and described how the invention solved them—and rejected the defendant's attempt at overgeneralizating the claims. *Id*.

The same applies here. Reading the claims in light of the specification which describes how the claimed inventions provide technological improvements over the prior art—e.g., "such that there is no need for the clock domain crossing circuit [thereby] eliminating a technical problem" ('381 patent 14:37-47)—and accepting these disclosures and the allegations in the Complaint as true—shows the claimed inventions are directed to technical improvements over conventional FPGA systems, not an abstract idea.

3. Defendant's Cited Cases Are Readily Distinguishable

None of Defendant's cases involves claims directed to specific improvements in computer technology. For example, in *Beteiro, LLC v. DraftKings Inc.*, the claims recited methods for "facilitating gaming activity and/or gambling activity." 104 F.4th 1350, 1353 (Fed. Cir. 2024). The specification admitted the claims were not aimed at solving computer-related problems but rather at making gambling more accessible. *Id.* The Federal Circuit thus found the claims analogous to a longstanding business activity: a casino accepting bets. *Id.* at 1356-57.

In *Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, the claims were directed to the conventional activity of communicating whether a garage door is open or closed—except wirelessly. 935 F.3d 1341, 1345-46 (Fed. Cir. 2019). The court found them abstract because they

offered nothing beyond the generic concept of wirelessly communicating information. *Id.* at 1346. In other words, as in *Beteiro*, the *Chamberlain* claims did not provide improvements in computer functionality, such as an improved way of wirelessly communicating the status information, but rather the abstract idea of wirelessly communicating status information itself. Similarly, in *ChargePoint, Inc. v. SemaConnect, Inc.*, the claims were directed to "wireless communication" in EV charging stations. 920 F.3d 759, 766–69 (Fed. Cir. 2019). The claims were deemed abstract because nothing in the patents indicated that "the charging station itself is improved from a technical perspective, or that it would operate differently than it otherwise could." *Id.* at 768.

By contrast, the patents here do not merely computerize a longstanding business activity or other known process. Rather, they aim to solve specific "technological challenges" such as reducing latency caused by CDC operations in conventional FPGA systems. And as shown above, the claims detail specific steps that require specific hardware elements configured to perform specialized operations in an unconventional, inventive and particular way. *See Adasa Inc. v. Avery Dennison Corp.*, 55 F.4th 900, 909 (Fed. Cir. 2022) (claims directed to "specific, hardware-based … structure designed to enable technological improvements" not abstract). Moreover, the claims do not remotely preempt all ways of performing clock-synchronized data processing or data manipulation; nor all uses of FPGAs or PLLs. *See Bascom*, 827 F.3d at 1350 (while filtering internet content was known, the patent described "how its particular arrangement of elements is a technical improvement" and thus did not "preempt all ways of filtering content on the Internet").

Defendant's heavy reliance on *Redwood Techs., LLC v. Netgear, Inc.*, 738 F. Supp. 3d 511 (D. Del. 2024) is also misplaced. The ineligible claims there related to wireless systems but unlike the claims here, did not recite "specific improvements" to such systems—and unlike the patents here, the *Redwood* patents did not explain how the claims advanced over the prior art. *Id.* at 519-20,

23-26; *see also* Factual Background. Moreover, unlike the specific circuitry called out in the claims here—e.g., "transmitting, from the ***deserializer*** to a ***phase lock loop … that is not within the [FPGA]***, the receiver side clock signal" ('381 claim 1, emphasis added)—the *Redwood* claims merely recited "result-based functional language." *Id.* at 519, 526.

4. Defendant's Other Arguments Fail

Defendant's assertion that the claims merely recite the functional results of "receiving," "generating," "converting," "transmitting," and "performing . . . operations" (Mot. at 8-9) improperly strips away the patents' claimed advances and should thus be rejected. *Compare* Mot. at 8-9 *with* Ex. 1; *see also* Factual Background. Such logic cannot be right, since contrary to Federal Circuit precedent, it leads to the improper conclusion that virtually all computer-related claims would be rendered ineligible when watered down to this degree. *See Uniloc*, 957 F.3d at 1309 (rejecting characterization of claims as mere "data manipulation"); *SRI*, 930 F.3d at 1304 (rejecting characterization of claims as "generic steps required to collect and analyze data"); *Packet Intelligence*, 965 F.3d at 1308 (rejecting oversimplification of claims as mere "collection, comparison, and classification of information").

Defendant's assertion that the claims do not specify "what type of 'operations' are involved, how they are performed, or what the 'computational circuitry' entails" (Mot. at 9) likewise misses the mark. Controlling precedent makes clear that under *Alice* step one, the Court must look at the claims *as a whole*—not individual steps/elements in isolation to determine whether each is abstract. *See Contour IP*, 113 F.4th at 1379; *Buffalo*, 2023 WL 5858921, at *4. Indeed, step one evaluates "what the *patent asserts* to be the focus of the claimed advance" as opposed to any isolated element(s) a defendant chooses to spotlight. *TecSec*, 978 F.3d at 1292.

Defendant's assertion that the claims are abstract because they utilize known components that do not have "any new capabilities" (Mot. at 9) also fails. Indeed, "employ[ing] known or

conventional components … does not necessarily mean that the claim is directed to an abstract idea." *Contour IP*, 113 F.4th at 1380; *see also Uniloc*, 957 F.3d at 1308-09 (rejecting argument that use of "generic Bluetooth components" rendered claims abstract); *Adasa*, 55 F.4th at 908 ("Setting aside the conventional RFID hardware components, claim 1 as a whole focuses on the data structure of the serial number space."). As in *Enfish*, this is not a situation where "general-purpose computer components are added post-hoc to a fundamental economic practice or mathematical equation." 822 F.3d at 1339. Rather, "the claims are directed to a specific implementation of a solution to a problem" in FPGA systems—the antithesis of abstract. *Id.*

Finally, Defendant's assertion that the claimed inventions "do not solve any technical problem relating to the use of [CDC] circuits" because they "avoid the use of [CDC] circuits altogether" is nonsensical. Mot. at 10. The inventor sought to address, e.g., latency issues caused by CDC circuits, and thus developed specific FPGA system designs that eliminate the need for such circuits—this alone establishes the claims are not abstract. *See* Factual Background.

* * *

Because the claims are not abstract, Defendant's motion should be denied. *CardioNet, LLC v. InfoBionic, Inc.*, 955 F.3d 1358, 1371 (Fed. Cir. 2020) (finding "district court erred by disregarding the written description's recitation of the advantages of the claimed invention.").

B. Defendant Fails to Show the Claims Lack an Inventive Concept Much Less by Clear and Convincing Evidence

Even assuming the asserted patents were directed to an abstract idea (they are not), Defendant's motion still fails because it cannot show that the claims lack an inventive concept.

1. Defendant Cannot Show the Patents Admit that the Claimed Inventions Were "Well-Understood, Routine, and Conventional"

"A Rule 12 motion to dismiss can only be resolved if the specification itself '***admits*** that the claim elements are well-understood, routine, and conventional.'" *Buffalo*, 2023 WL 5858921,

at *4 (citing *Riggs Tech. Holdings, LLC v. Cengage Learning, Inc.*, No. 2022-1468, 2023 WL 193162, at *4 (Fed. Cir. Jan. 17, 2023)). The specification here does nothing of the sort. To the contrary, it discloses that the claimed inventions depart from well-understood, routine, and conventional FPGA systems—for example, by using an external PLL to synchronize receiver- and transmitter-side clock signals, and avoiding clock domain crossing operations that delay processing. *See* Factual Background. The patents thus amount to "significantly more" than an abstract idea. *See Cooperative*, 50 F.4th at 131–32) (inventive concept where patent "explains how [claimed] network structure is different from and improves upon the prior art").

2. Defendant's "Generic Components" Arguments Misread the Patents and the Law

Defendant's assertion that the claims lack inventive concept because they utilize "generic and conventional components" (Mot. at 11) is meritless. Indeed, an "[i]nventive concept can be found in the non-conventional and non-generic arrangement of known, conventional pieces." *Bascom*, 827 F.3d at 1350; *see also Cooperative*, 50 F.4th at 135 ("useful improvements to computer networks are patentable regardless of whether the network is comprised of standard computing equipment"). Here, the patents plainly disclose that the particular arrangement of claim elements was unconventional, which the Court must accept as true. *See* Factual Background; *Bergman Healthcare Pty. Ltd. v. Seneca Sense Techs. Inc.*, No. 1:22-CV-02167, 2023 WL 6388147, at *6-7 (N.D. Ill. Sept. 30, 2023) (statements in pleadings and intrinsic record identifying "specific ways in which the [p]atent unconventionally improves upon prior art 'to improve efficiency'" preclude dismissal at the pleading stage).

Defendant's reliance on purported admissions that certain individual components such as FPGAs and PLLs were commercially available highlights the error in its analysis. Mot. at 12-13. The patents do not claim to invent FPGAs or any other individual component, nor the "invocation

of market data." Rather, the patents describe and claim new system architectures that, e.g., eliminate CDC operations—this alone constitutes an inventive concept (even if generic FPGA components are used). In other words, the claimed inventive concepts lie in the unconventional arrangements and configurations of hardware elements and their unique interactions.

Thus, even assuming the claims were drawn to the abstract idea of "synchronizing data processing with a clock" or "data manipulation" (they are not), the claims remain patent-eligible because they present a concrete solution with "the specificity required to transform a claim from one claiming only a result to one claiming a way of achieving it." *Interval Licensing*, 896 F.3d at 1343 (internal citation omitted); *see also Weisner v. Google LLC*, 51 F.4th 1073, 1085-86 (Fed. Cir. 2022) (district court erred in relying on patent statements conceding patentee did not invent new search engine because the claims "do not per se concern searching for new information, but rather concern a new technique for prioritizing the results of the conventional search"). The highlighted elements in Exhibit 1 go well beyond mere data synchronization or manipulation but detail "how" the claimed inventions reduce latency using an inventive, unconventional arrangement of circuitry. Thus, the claims "add significantly more" to any purported "abstract idea by implementing a specific solution to a problem rooted in computer technology." *Id*. at 1088.

3. Rule 12(b)(6) and Questions of Fact Compel Denial

Even if the Court were to give credence to Defendant's unsupported attorney argument, this at best creates fact issues precluding dismissal. See *Buffalo*, 2023 WL 4594945, at *8 ("[A]t the very least there are factual disputes regarding whether the patents contain an inventive concept which would preclude granting Motorola's motion [to dismiss].") Thus, at minimum, the Court should deny Defendant's motion to dismiss because "determining whether the claimed [invention] is well-understood, routine, or conventional is a question of fact that cannot be resolved at the Rule 12(b)(6) stage." *Cooperative*, 50 F.4th at 133. Courts in this District have properly

denied dismissal under similar facts. *See, e.g.*, *Buffalo*, 2023 WL 5858921, at *4 ("At a minimum there is a factual dispute about whether the asserted patents involve components performing well-understood, routine, conventional activities"); *Disintermediation*, 2024 WL 2209709, at *4. ("Plaintiff has alleged facts to state a plausible claim that the patented technology includes an inventive concept" where plaintiff alleged that the patents address a "technological problem and involve an inventive concept"). Alternatively, Plaintiff should be granted leave to amend its Complaint. *Aatrix Software, Inc. v. Green Shades Software, Inc.*, 882 F.3d 1121, 1126 (Fed. Cir. 2018) ("[I]t was an abuse of discretion for the district court to deny leave to amend.").

C. Defendant Fails to Show Any Claim Is Representative

Defendant asserts that '381 claim 1 and '286 claim 1 "are representative of the patents as a whole" because they "closely resemble each other and are based on the same abstract idea." But even a cursory glance at those claims alone shows they do not resemble each other. *See* Ex. 1. And the purported "same abstract idea" is Defendant's egregious oversimplification of the claims, as discussed above. Further, it is Defendant's burden to prove invalidity by clear and convincing evidence and conclusory attorney argument that a claim is representative of all claims in all patents is a far cry from meeting that burden.

Likewise, for the dependent claims, Defendant continues its charade of mischaracterizing claim elements as mere "data manipulation." Mot. at 15. As shown in Exhibit 2, at least the highlighted dependent claim elements relate to the patents' patent-eligible technological improvements that help reduce latency in conventional FPGA systems, e.g., by eliminating the need for conventional CDC circuits and operations.

V. CONCLUSION

For the foregoing reasons, Defendant's motion to dismiss should be denied.

Dated: May 5, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on May 5, 2025, I electronically filed the foregoing document with the Clerk of the Court for the Northern District of Illinois using the ECF System which will send notification to the registered participants of the ECF System as listed on the Court's Notice of Electronic Filing.

/s/ *Dale Chang*
Dale Chang